ore	0.5 3573
X	98

Home | Login | Logout | Access Information | Alerts |

D Search Results

IEEE XPLORE GUIDE Welcome United States Patent and Trademark Office SEARCH

BROWSE

Results for "(parameter<in>metadata } <and> (delay model<in>metadata)"

Your search matched 110 of 1192192 documents. A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

<u>.</u>

Citation & Abstract

View: 1-25 | 26-5

â

model<in>metadata

sults set

with accurate delay models for core-based designs ity Electronic Design, 2003. Proceedings. Fourth International Symposium on March 2003 Page(§):319 - 324 AbstractPlus | Full Text: PDE(2881 KB) | IEEE CNF

A comprehensive delay model for CMOS inverters Solid-State Circuits, IEEE Journal of Volume 30, Issue 8, Aug. 1995 Page(s):864 - 871 Dutta, S.; Shetti, S.S.M.; Lusky, S.L.;

AbstractPlus | Full Text: PDE(676 KB) | IEEE JNL

Oliveira, A.L.; Murgei, R.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 22, Issue 6, June 2003 Page(s):907 - 814 On the problem of gate assignment under different rise and fall delays AbstractPlus | References | Full Text: PDE(509 KB) Ľ

Delay modeling and timing of bipolar digital circuits Saab, D.C., Yang, A.T., Haji, I.N., Design Automation Conference, 1988. Proceedings., 26th ACM/IEEE 12-15 June 1988 Page(s):288 - 293 AbstractPlus | Full Text: PDE(480 KB) | IEEE CNF 二

Circuits and Systems, 1989., IEEE International Symposium on Generic linear RC network model for digital CMOS circuits AbstractPlus | Full Text: PDE(320 KB) IEEE CNF 8-11 May 1989 Page(s):860 - 863 vol.2 Deng, A.C.; Shiau, Y.C.; Ш

BICMOS gate performance optimization using a unified delay model Raje, P.; Cham, K.; Saraswat, K.; VLSI Technology, 1990. Digest of Technical Papers, 1990 Symposium on AbstractPlus | Full Text: PDE(160 KB) IEEE CNF 4-7 June 1990 Page(s):91 - 92 φ Ľ

7/6/2005 http://ieeexplore.ieee.org/search/searchresult.jsp?query1=parameter&scope1=metadata&op...

http://ieeexplore.ieee.org/search/searchresult.jsp?query1=parameter&scope1=metadata&op... 7/6/2005

AbstractPlus | References | Full Text: PDE(358 KB) | IEEE JNL

AUTODDM: automatic characterization tool for the detay degradation model blanchico, J. Befilio, M.J., Ruiz-declarido, P.; Beena, C.; Valenda, M.; Electronics, Circuits and Systems, 2001. (CECS 2001. The 8th IEEE International Control Volume 3, 2-5 Sept. 2001 Page(s):1631 - 1634 vol.3 Efficient core designs based on parametentzed macrocells with accurate delay m Mansour, M.M.; Mehrotra, A.; Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Sympos Volume 5. 25-28 May 2003 Page(s):V-517 · V-520 vol.5 10. In-fiber grating systems for pulse compression and complete dispersion comper Williams, J.A.; Sugden, K.; Zhang, L.; Bernhon, I.; Oorna, N.J.; Optical Fiber Gratings and Their Applications, IEE Colloquium on 30 Jan 1995 Page(s):9/1 - 9/6 An accurate analytical propagation delay model for high-speed CML bipolar circi Sharaf, K.M.; Elmasry, M.I.; Sizing an inverter with a precise delay: generation of complementary signals with and pulsewidth distortion in CMOS Xiaodong Yang; Ku, W.H.; Chung-Kuan Cheng; Computer-Aided Design, 1999. Digest of Technical Papers. 1999 IEEE/ACM Internatio Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [and Systems I: Regular hepsex, IEEE Transactions on Journal Sol, Issue 4, April 2003 Page(s):572 - 575 7. RLC interconnect delay estimation via moments of amplitude and phase respons Propagation delay model of a current driven RC chain for an optimized design Patumbo, G.; Poll, M.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 10, Issue 5, May 1991 Page(s):577 - 588 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 8, Issue 1, Jan. 1989 Page(s):33 - 40 Circuits and Systems for Video Technology, IEEE Transactions on An accurate analytical detay model for BICMOS driver circuits Diaz, C.H.; Kang, S.-M.; Leblebici, Y.; 11. Asymptotic limits of video signal processing architectures AbstractPlus | Full Text: PDE(1684 KB) | IEEE JNL AbstractPlus | Full Text: PDE(1068 KB) IEEE JNL AbstractPlus | Full Text: PDE(352 KB) IEEE CNF AbstractPlus | Full Text: PDE(436 KB) IEEE CNF AbstractPlus | Full Text: PDE(464 KB) | IEEE CNF AbstractPlus | Full Text: PDE(956 KB) | IEEE JNL AbstractPlus | Full Text: PDE(660 KB) | IEEE JNL AbstractPlus | Full Text: PDE(352 KB) IEE CNF Volume 5, Issue 6, Dec. 1995 Page(s):545 - 561 Volume 29, Issue 1, Jan. 1994 Page(s):31 - 45 Solid-State Circuits, IEEE Journal of 7-11 Nov. 1999 Page(s):208 - 213 Dutta, S.; Wolf, W.; Argade, P.V.; Ü L Ľ L Ľ Ш Ľ L

IEEE Xplore# Search Result	Page 3 of 4 traveling-wave-based waveform approximation technique for the timing verific transmission lines Yungsoon Ed. Jongin Shim: Elsenstadt, W.R.; Computer Ed. Jongin Shim: Elsenstadt, W.R.; Computer St., Issue 6, June 2002 Page(s):723 - 730 AbstractPlus References Full Text: EDE(471 KB) EEE JNL	Page 3 of 4 imation technique for the timing verific and systems, IEEE Transactions on 3-730
C	17. Adaptive proportional delay differentiated services: characterization and perform Leung, MK.Hr.; Lui, J.C.S.; Yau, D.K.Y.; Networking, IEEE/ACM Transactions on Volume 9, Issue 6, Dec. 2001 Page(s):801 - 817 Abstract	I services: characterization and perform -817 99 KB) IEEE JNL
	18. Transiting alroraft parameter estimation using underwater acoustic sensor data Ferguson, B.G.; Lo, K.W.; Coeanic Engineering, IEEE Journal of Volume 24, Issue 4, Oct. 1999 Page(s):424 - 435 AbstraciPlus References Full Text. PDE(568 KB) IEEE JNI.	ising underwater acoustic sensor data 1 - 435 68 KB) IEEE JNL
Ľ	19. An analytical delay model for RLC interconnects Kahng, A.B.; Muddu, S.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 16, Issue 12, Dec., 1997 Page(s);1507 - 1514 AbstractPlus References Full Text.	nnacts 1s and Systems, IEEE Transactions on 507 - 1514 112 KB) IEEE JNL
	20. A spread spectrum communications channel sounder Austin, J.; Ditmar, W.P.A.; Wal Keung Lam; Vilar, E.; Kin Wa Wan; Communications, IEEE Transactions on Volume 45, Issue 7, July 1997 Page(s):840 - 847 AbstractPlus References Full Text. PDE(216 KB) IEEE JNL	nnel sounder Vilar, E.; Kin Wa Wan;) - 847 216 KB) IEEE JNL
	21. Adaptive control of dominant time delay systems via polynomial identification Besharati Rad, A., Tsang, K.M.; Lo, W.L.; Control Theory and Applications, IEE Proceedings-Volume 142, Issue 5, Sept. 1995 Page(s):433 - 438 AbstraciPlus Full Text: PDE(308 KB) IEE JNL.	systems via polynomial identification edings- 133 - 438 JNL
	22. Process characterisation with dynamic test structures Coli, P.; Robert, M.; Reginer, X.; Auvergne, D.; Electronics Letters Volume 29, Issue 20, 30 Sept. 1993 Page(s):1764 - 1766 AbstractPlus Full Text: PDE(236 KB) IEE JML	lic test structures yne, D.; agge(s):1764 - 1766 IEE JNL
ם	23. Analytical approach to sizing nFET chains Bizzan, S.S., Jullien, G.A.; Miller, W.C.; Electronics Letters Volume 28, Issue 14, 2 July 1992 Page(s):1334 - 1335 AbsitaciPlus Fulf Text: PDE(148 KB) IEE JNL	1334 - 1335 Juli
e	24. Analytical dynamic time delay model of strongly coupled RLC interconnect lines switching service of the sensity of the sen	strongly coupled RLC interconnect lines W.R.; Jongin Shim; js. 5th international Symposium on
Ľ	25. Critical path issue in VLSI design	

http://ieeexplore.ieee.org/search/searchresult.jsp?query l=parameter&scope1=metadata&op... 7/6/2005

IEEE Xplore# Search Result

Page 4 of 4

Youssel, H.; Shragowitz, E.; Bening, L.; Computer-Added Design, 1989. ICCAD-89. Digest of Technical Papers., 1989 IEEE Into Conference on 5-9 Nov. 1989 Page(8):520 - 523 AbstractPlus | Full Text: DDE(332 KB) | IEEE CNF

View: 1-25 | 26-5

Help Contact Us Privacy &

• Copyright 2005 IEEE -

http://ieeexplore.ieee.org/search/searchresult.jsp?query1=parameter&scope1=metadata&op... 7/6/2005

OFE"	
Ypl	
33	

Home | Login | Logout | Access Information | Alerts | Welcome United States Patent and Trademark Office

C Search Results

IEEE XPLORE GUIDE SEARCH

Results for "[parameter<in>metadata | cellag model<in>metadata |"
Your search matched 110 of 1192182 documents.
A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

2	Modity Search [parameter-cin-pretadata) <and> (delay model<n-> (delay model<n-> (delay model<n-> (delay model<n-> (delay model<n-> (delay model<n-> (delay model Check to search only within this results set</n-></n-></n-></n-></n-></n-></and>	b View.Session.Listory b New Search b Key IEEE JNI, IEEE Journal or Megazine IEE INL IEE Journal or Megazine CNF Proceeding IEEC Conference CNF Proceeding	New.Sear New.Sear Rey EEE JNL IEEE JNL IEEE CNF
-	%	IEE Conference Proceeding	IEE CNF
		(EEE Conference Proceeding	CNF
Select			IEE JNL
Select	Display Format: 6 Citation C. Citation & Abstract	, IEEE Journal or Magazine	
Displa Select	Check to search only within this results set		e Key
Oispla Select	(parameter <in>metadata) <and> (delay model<in>metadata)</in></and></in>		Š
Oispla	Modify Search	ED.	New Sear
Modify [perar] Ch Displa Select		sion History	View Ses

OS driver circuits Symposium on

View: 1-25 | 26-5

â

AbstractPlus | Full Text: PDE(360 KB) | IEEE CNF

Military Communications Conference, 1992. MILCOM '92, Conference Record. 'Comm 27. Time-of-arrival measurement for transionospheric EMP Fusing Command, Control and Intelligence'., IEEE 11-14 Oct. 1992 Page(s);1058 - 1061 vol.3 AbstractPlus | Full Text: PDE(316 KB) IEEE CNF Ľ

Delay modelling and optimization of BiCMOS buffer circuits Eson, M.O.; A-Khraili, D.; A-Khraili, A.J.; Circuits and Systems, 1993, Proceedings of the 36th Midwest Symposium on 16-18 Aug. 1993 Page(s):566 - 569 vol.! AbstractPlus | Full Text: PDE(424 KB) | IEEE CNF Ш

Towards incorporating device parameter variations in timing analysis Siveraman, M.; Sairojwas, A.J.;
European Design and Test Conference, 1994. EDAC, The European Conference on D ETIC European Test Conference. EUROASIC, The European Event in ASIC Design, Pp. 28 Feb.-3 March 1994 Page(s):338 - 342 23 Ľ

AbstractPlus | Full Text: PDE(448 KB) | IEEE CNF

30. Accurate technology Independent models for submicron CMOS and BICMOS cin Cocchini, P.; Piccinini, G.; Zamboni, M.; Electrotechnical Conference, 1996. MELECON '96., 8th Mediterranean Volume 3, 13-16 May 1996 Page(s):1267 - 1270 vol.3 AbstractPlus | Full Text: PDE(336 KB) | IEEE CNF Ľ

Abe, N.; Seki, K.; Kanoh, H.; Industrial Electronics, 1996. ISIE '96., Proceedings of the IEEE International Symposiu Volume 1, 17-20 June 1996 Page(s):260 - 265 vol.1 31. Two degree of freedom internal model control for single tubular heat exchanger: AbstractPlus | Full Text: PDE (588 KB) IEEE CNF C

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

Huang Lingyi, Zhu Ualjang; Qiu Yuling; Ye Qing; Chen Chaoshu; Chen Xiaodong; Su Z Zhao; Wang Yuhui; Chen Xia; Solid-State and Integrated Circuit Technology, 1998. Proceedings, 1998 5th Internation 21-23 Oct. 1998 Page(s):505 - 508 Fujita, T.; Onodera, H.; Circuits and Systems, 2000. Proceedings, ISCAS 2000 Geneva. The 2000 IEEE Intern 38. Characterization and performance evaluation for proportional delay differentiate Circuits and Systems, 1996. ISCAS '96.. 'Connecting the World'., 1996 IEEE Internation 40. Variable length packet switches: delay analysis of crossbar switches under Pois Manjunath, D.; Sikdar, B.; INFOCOM 2000. Nineteenth Annual Joint Conference of the IEEE Computer and Com 35. A high speed base library and macro library design methodology for submicron Oliveira. A.L.; Murgail. R.; Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on 5-9 Nov. 2000 Page(s):451 - 457 39. An exact gate assignment algorithm for tree circuits under rise and fall delays Multi-Chip Module Conference, 1996. MCMC-96, Proceedings., 1996 IEEE Leung, M.K.H.; Lui, J.C.; Yau, D.K.Y.; Network Protocols, 2000. Proceedings. 2000 International Conference on 14-17 Nov. 2000 Page(s):295 - 304 36. Characterizing individual gate power sensitivity in low power design Narayanan, U.; Stamoulis, G.I.; Rdy, R.K.; VLS) Design, 1998. Proceedings. Tweith International Conference On 7-10 Jan. 1999 Page(8):625 - 628 Verilog HDL Conference, 1995. Proceedings., 1995 IEEE International 27-29 March 1995 Page(s):49 - 55 33. Efficient gate delay modeling for large interconnect loads 37. Statistical delay calculation with vector synthesis model An analytical delay model for RLC interconnects Kahng, A.B.; Muddu, S.; Volume 4, 12-15 May 1996 Page(s):237 - 240 vol.4 Volume 5, 28-31 May 2000 Page(s):473 - 476 vol.5 AbstractPlus | Full Text: PDE(424 KB) IEEE CNF AbstractPlus | Full Text: PDE (336 KB) IEEE CNF AbstractPlus | Full Text: PDE(284 KB) IEEE CNF AbstractPlus | Full Text: PDE(492 KB) | IEEE CNF AbstractPlus | Full Text: PDE(124 KB) | IEEE CNF AbstractPlus | Full Text: PDE(108 KB) | IEEE CNF AbstractPlus | Full Text: PDE(616 KB) IEEE CNF AbstractPlus | Full Text: PDE(704 KB) IEEE CNF 34. Standardizing delay calculation in Verilog 6-7 Feb. 1996 Page(s):202 - 207 submicron ULSi similar traffic Ľ Ľ Ц Ĺ L \Box Ľ L L

IEEE Xplore# Search Result	Page 3 of 4
	Societies, Proceedings, IEEE Volume 2, 26-30 March 2000 Page(s):1055 · 1064 vol.2 AbstractPlus Full Text: DDE(828 KB) IEEE CNF
	41. Using the boundary scan delay chain for cross-chip delay measurement and cha delay modeling flow Schmid. J.; Schuring, T.; Smala, C.; Schmid, J.; Schuring, T.; Smala, C.; Quality Electronic Design, 2001 International Symposium on 26-28 March 2001 Page(s):337 - 342 AbstractPlus Full Text: DDE(554 KB) IEEE CNF
Ľ	42. Impact of power-supply noise on timing in high-frequency microprocessors Saint-Laurent, M.; Swaminathan, M.; Electrical Performance of Electronic Packaging, 2002 21-23 Oct. 2002 Page(6):261 - 264 AbstractPlus Full Text: PDE(393 KB) IEEE CNF
	43. On the robustness of linear delayed systems with nonlinear uncertain parameter Jato Sun; Yinping Zhang; Irraligent Control and Automation, 2002. Proceedings of the 4th World Congress on Volume 4, 10-14 June 2002 Page(s):3085, 3087 vol.4 Abstradizius Fuil Text: PDE(300 KB) IEEE CNF
0	44. An efficient approach for the selection of priority control parameters in adaptive delay differentiated services Chongot Feng, Pingy Feng. Tear. Yicheo Wang; Ning Ge; Personal, Indoor and Mobile Radio Communications, 2003. PIMRC 2003. 14th IEEE P Volume 1, 7-10 Sept. 2003 Page(s):89 - 104 Vol.1 AbstractPlus Fuil Text: DDE(62 1 KB) IEEE CNF
6	45. A wideband channel model applicable to mobile satellite systems at L- and S-bar Parks, M.An., Saunders, S.R.; Evans, B.G.; Propagation Aspects of Future Mobile Systems (Digest No: 1996/220), IEE Colloquium 25 Oct, 1996 Page(s):1211-126 AbstractPlus Fuil Text: PDE(348 KB) IEE CNF
C	46. Time-of-arrival prediction model for transionospheric EMP Kim, Y.S., Eng, R.; Aerospace and Electronic Systems, IEEE Transactions on Volume 31, Issue 1, Jan 1995 Page(s):409 - 413 AbstractPlus Full Text: PDE(284 KB) IEEE JAIL
<u> </u>	47. Simulation of high speed interconnects using a convolution-based hierarchical fundator Shael, M.S.; Steer, M.B.; Franzon, P.D.; Components, Perdaging, and Manufacturing Technology, Part B: Advanced Packaging, Transactions on (see also Components, Hyprids, and Manufacturing Technology, IEEE Volume 18, Issue 1, Feb. 1995 Page(8):74 - 82 AbstractElus Full Text: EDE(776 KB) IEEE JNL
Ľ	48. Blood pressure control during surgical operations Fundani, E., Araki, M.; Maelani, S.; Blomedical Enginearing, IEEE Transactions on Volume 42, Issue 10, Oct. 1995 Page(s):999 - 1006 Abstradizius Full Text: DDE(664 KB) IEEE JNL
	49. Switch-level timing simulation of bipolar ECL circuits

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

IEEE Xplore# Search Result

Page 4 of 4

Yang, A.T.; Chang, Y.-H.; Saab, D.G.; Halj, I.N.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 12, Issue 4, April 1933 Page(s);516 - 530
AbstractDus | Fulf Text: DDE(1204 KB) | IEEE JNL

Ľ

50. Performance of synchronous and asynchronous schemes for VLSI systems Alghabi, M.; Svensson, C.; C.; Computera, IEEF Transactions on Volume 41, Issue 7, July 1992 Page(4):858 - 872
AbstractPlus | Full Text: PDE(1424 KB) | IEEE Jul.

View: 1-25 | 26-5

& Copyright 2005 IEEE -

Help Contact Us Privacy &.

Indexed by

ore	
ľďX	
3 5	

C Search Results

Home | Login | Logout | Access Information | Alerts |

Office	
Trademark	
atent and	
d States P	
ome Unite	
Welco	

BROWSE SEARCH IEEE XPLORE GUIDE

. Marian

Results for "[parameter≺in>metadata] <and> (delay model<in>metadata]" Your search matched 110 of 1192192 documents. A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

	Modify Search	(parameter <in>metadata) <and> (delay model<in>metadata)</in></and></in>	Check to search only within this results set	Display Format: (6) Citation C. Citation & Abstract		Select Article Information	51. Accurate delay models for digital BiCMOS Raje, P.A.; Saraswat, K.C.; Cham, K.M.;	Electron Devices, IEEE Transactions on Volume 39, Issue 6, June 1992 Page(s):1456 - 1464	AbstractPlus Full Text: PDF(732 KB) IEEE JNL
,	ion History			IEEE JNL (EEE Joumal or Magazine	IEE JNL IEE Journal or Magazine	IEEE Conference Proceeding	IEE CNF IEE Conference Proceeding	IEEE Standard	
	 View Session History New Search 		» Key	IEEE JNL	IEE JNL	CNF	IEE CNF	STO	

View: 1-25 | 26-5

52. Performance-driven scaling of BICMOS technology
Raje, P.A.; Sarawati, K.C.; Oham, K.M.;
Electron Devices, IEEE Transactions on
Volume 39, 1ssue 3, March 1992 Page(s):885 - 694
AbstractPlus | Fuil Text: DDE(648 KB) | IEEE JNL

53. Generic linear RC delay modeling for digital CMOS circuits
Deng, A.-C.; Shiau, Y.-C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 9, Issue 4, April 1990 Page(s):367 - 376
AbstractPlus | Full Text; EDE(818 KB) | IEEE JNL

64. Fitted Elmore delay: a simple and accurate interconnect delay model Abou-Seido, Al.; Nowak, B.; Chu, C.; Very, Large Scale integration (VLSI) Systems, IEEE Transactions on Volume 12, Issue 7, July 2004 Page(s):691 - 696
AbstractClus | References | Full Text. PDE(296 KB) | IEEE JNL

55. Impact of power-supply noise on timing in high-frequency microprocessors
Saint-Laurent, M.; Swaminathan, M.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging and M. Technology and B. Advanced Packaging, IEEE Transactions on]
Volume 27, issue 1, Fab. 2004 Page(s);135 - 144
AbstractDus | References | Full Taxt: PDE(696 KB) | IEEE JNL

56. A delay model for router microarchitectures
L-Shiuan Peh; Dally, W.J.;
Micro, IEEE
Micro, IEEE
Volume 21, Issue 1, Jan.-Feb. 2001 Page(s):28 - 34
AbstractDlus | References | Full Toxt: EDE(128 KB) | IEEE JNL

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [i and Systems II: Express Briefs, IEEE Transactions on] Volume 47, Issue 5, May 2000 Page(5):452 - 461 An analytic model for the design and optimization of ion-implanted I/SUP 2/L dev Evans, S.A.; 65. Switching activity estimation under real-gate delay using timed Boolean function Theodordial, 6.; Theohafs, 5.; Soudis, D.; Gordis, C.; Computers and Digital Techniques, IEE Proceedings-Volume 147, Issue 6, Nov. 2000 Page(s):444 - 450 Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [64. Optimal control of a coupled-core nuclear reactor by a singular perturbation met 62. Automatic netlist extraction for measurement-based characterization of off-chip 61. Modeling of gate line deby in very large active matrix liquid crystal displaye Ging Zhang: Shen. D.S. Gleskova, H.: Wagner, S.; Electron Devices, IEEE Transactions on 57. Modeling and optimized design of current mode MUX/XOR and D flip-flop 58. Peak power estimation of VLSI circuits: new peak power measures Hsiao, M.S.; Rudnick, E.M.; Petel, J.H.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on AbstractPlus | References | Full Text: PDE(148 KB) | IEEE JNL 59. Analysis and optimization of a uniform long wire and driver Fenghao Mu; Svensson, C.; 60. Response-time properties of linear asynchronous pipelines Ebergen, J.; Berks, R.; AbstractPlus | References | Full Text: PDE(212 KB) | IEEE JNL AbstractPlus | References | Full Text: PDE(472 KB) | IEEE JNL AbstractPlus | References | Full Text: PDE (392 KB) | IEEE JNL AbstractPlus | References | Full Text: PDE(164 KB) | IEEE JNL AbstractPlus | References | Full Text: PDE(92 KB) | IEEE JNL Corey, S.D.; Yang, A.T.; Microwave Theory and Techniques, IEEE Transactions on Volume 45, Issue 10, Oct. 1997 Page(s):1934 - 1940 and Systems I: Regular Papers, IEEE Transactions on) Volume 46, Issue 9, Sept. 1999 Page(s):1086 - 1100 Proceedings of the IEEE Volume 87, Issue 2, Feb. 1999 Page(s):308 - 318 AbstractPlus | Full Text: PDE(1176 KB) | IEEE JNL Reddy, P.: Sannuti, P.: Automatic Control, IEEE Transactions on Volume 20, Issue 6, Dec 1975 Page(s):766 - 769 Volume 45, Issue 1, Jan. 1998 Page(s):343 - 345 Solid-State Circuits, IEEE Journal of Volume 12, Issue 2, Apr 1977 Page(s):191 - 198 AbstractPlus | Full Text: PDE(440 KB) | IEEE JNL Volume 8, Issue 4, Aug. 2000 Page(s):435 - 439 AbstractPlus | Full Text: PDE(512 KB) REE JNL Alioto, M.; Palumbo, G.; Ľ Ľ L L L L L Ľ L

4		=			,		ē.	Œ	a 5
Page 3 of	66. Generalised Elmore delay expression for distributed RC tree networks Yamakoshi, K.; Ino, M.; Yamatconics Letters Electronics Letters Volume 29, Issue 7, 1 April 1993 Page(s):617 - 618 AbstractDus Full Text; PDE(196 KB) IEE JNIL	67. Power dissipation models and performance improvement techniques for CMOS i line and tree interconnections frang. HC.; Shalu, MC.; Circuits, Devices and Systems. IEE Proceedings G Volume 140, Issue 6, Dec. 1933 Page(s),437 - 443 AbstractDius Full Text: PDE(396 KB) IEE JNI.	68. Low power testing by test vector ordering with vector repetition Belios, M.; Bakalis, D.; Nikolos, D.; Karouslanos, X.; Quality Electronic Design, 2004. Proceedings. 5th International Symposium on 2004 Page(s):205 - 210 AbstractPlus Full Text: PDE(259 KB) IEEE CNF	69. Proposal of a timing model for CMOS logic gates driving a CRC /spi pil load Hirata, A.; Onodera, H.; Tamaru, K.; Computer-Aded Design, 1998, ICCAD 98. Digest of Technical Papers, 1998 IEEE/ACI Conference on B-12 Nov 1998 Page(s):337 - 544 AbstractPlus Full Text: PDE(548 KB) IEEE CNF	70. Static transition probability analysis under uncertainty Garg, S.; Tata, S.; Aumathalam, R.; Computer Delagin; VLS1 in Computers and Processors, 2004. ICCD 2004. Proceedings International Conference on 11-13 Oct. 2004 Page(s):380 - 386 AbstractPlus Full Text: PDE(298 KB) IEEE CNF	71. Simple approximation models for coupled RC lines with application to delay and estimation Ogata. M. Nishi, T.; Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on Volume 1, 25-28 July 2004 Page(s):1 - 409-12 vol.1 AbstractPlus Full Text: PDE(414 KB) IEEE CNF	72. Technology portable delay model for DSM CMOS inverters Kabbani, A.; ArKhalii, D.; ArKhalii, A.J.; Circuits and Systems, 2004. NEWCAS 2004. The 2nd Annual IEEE Northeast Worksh 20-23 June 2004 Page (8):13 - 16 AbstractPlus Full Text: PDE (353 KB) IEEE CNF	73. Astrometric VLBI observation of spacecraft with phase delay Sekido, M.; Ichikawa, R.; Osaki, I.; Kondo, T.; Koyama, Y.; Yoshikawa, M.; Ohnishi, T.; Novikov, A.; Benbue, M.; Radio Seince Conference, 2004. Proceedings. 2004 Asia-Pacific 24-27 Aug. 2004 Page(s):310 - 313 AbstractBlus Full Text: PDE(1886 KB) IEEE CNF	74. Gain acheduling control for electro-hydraulic servo system considering time-delerror Takahiro, S.; Kenko, U.; Control Applications, 2004. Proceedings of the 2004 IEEE International Conference on
IEEE Xplore# Search Result		C	D	С	□	C		C: .	C :
IEEE Xplore									

Page 4 of 4

AbstractPlus | Full Text: PDE(753 KB) IEEE CNF

Ü

75. Logical effort analysis of multi-port register file architectures
Burgess, N.;
Signals, Systems and Computers, 2003. Conference Record of the Thirty-Seventh Asil
on
Volume 1, 9-12 Nov. 2003 Page(s):887 - 891 Vol.1
AbstractPlus | Full Text: PDE(405 KB) | EEE CNF

View: 1-25 | 26-5

Help Contact Us Privacy &

© Copyright 2005 IEEE -

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005

http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=+%28+parameter%3Cin%3Em... 7/6/2005